MULTICUBE

Project Coordinator
Name: Cristina Silvano
Institution: Politecnico di Milano
Email: silvano@elet.polimi.it

Project website:
www.multicube.eu

Partners:
Politecnico di Milano (Italy),
Design of Systems on Silicon – DS2 (Spain),
STMicroelectronics (Italy),
IMEC (Belgium),
ESTECO (Italy),
University of Lugano - ALaRI (Switzerland),
University of Cantabria (Spain),
STMicroelectronics Beijing (China),
Institute of Computing Technology – Chinese Academy of Sciences (China)

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SEVENTH FRAMEWORK PROGRAMME

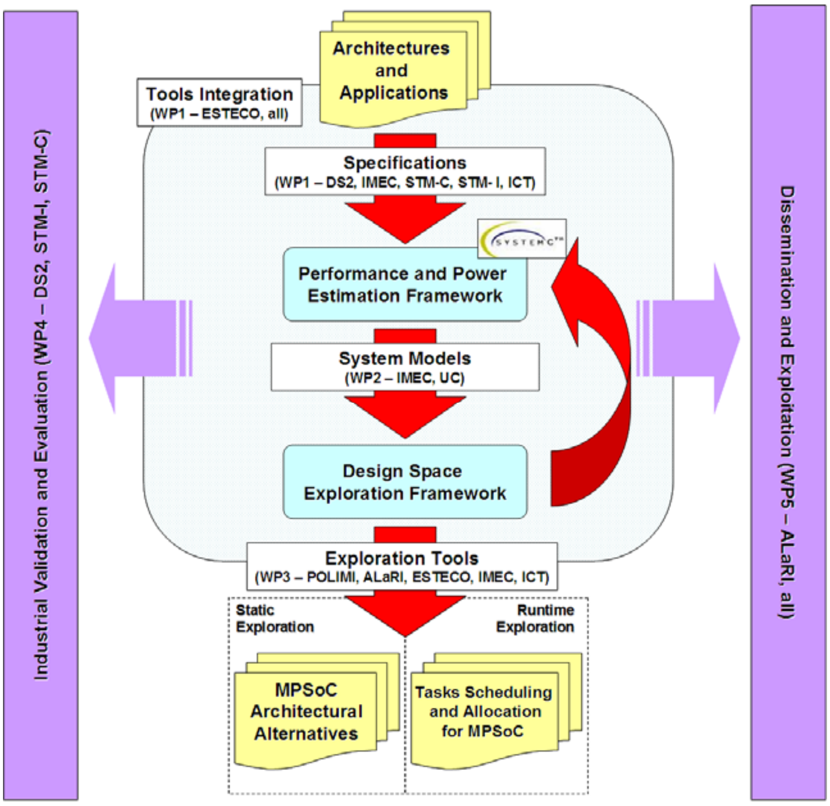
MULTICUBE

MULTI-OBJECTIVE DESIGN SPACE EXPLORATION OF MULTI-PROCESSOR SOC ARCHITECTURES FOR EMBEDDED MULTIMEDIA APPLICATIONS

Many point tools exist to optimise particular aspects of embedded systems. However, an overall design space exploration framework is needed to combine all the decisions into a global search space, and a common interface to the optimisation and evaluation tools. The MULTICUBE project focused on the definition of an automatic multi-objective Design Space Exploration (DSE) framework to be used to tune the System-on-Chip architecture for the target application evaluating a set of metrics (e.g. energy, latency, throughput, bandwidth, QoS, etc.) for the next generation of embedded multimedia platforms.

From one side, the MULTICUBE project defined an automatic multi-objective DSE framework to find design tradeoffs that best meet system constraints and cost criteria, strongly dependent on the target application, but also to restrict the search space to crucial parameters to enable an efficient exploration. In the developed DSE framework, a set of heuristic optimisation algorithms have been defined to reduce the overall exploration time by computing an approximated Pareto set of configurations with respect to the selected figures of merit. Once the approximated Pareto set has been built, the designer can quickly select the best system configuration satisfying the constraints.

From the other side, the MULTICUBE project defined a run-time DSE framework based on the applications of the results of the design-time multi-objective design exploration to optimise at run-time the allocation and scheduling of different application tasks. The design exploration flow results in a Pareto-optimal set of design tradeoffs with different speed, energy, memory and communication bandwidth parameters. This information can be used at run-time by the operating system to make an informed decision about how the resources should be distributed over different tasks running on the multi-processor system on-chip. This resource distribution cannot be done during the design exploration itself, since it depends on which tasks are active at that time.



MULTICUBE tool environment and design flow linked to the five workpackages

The goal of MULTICUBE was to cover the gap between the system-level specification and the definition of the optimal application-specific architecture. MULTICUBE activities are driven by the idea to cover this gap by building a set of tools and accurate methodologies directly targeted to specific multi-core architectures. In the MULTICUBE design flow, the specifications of the target architectures and applications will be provided as inputs to the design flow.
A SystemC-based multi-level modelling methodology for multiprocessors has been developed. Once received the target architecture as input, the system model is provided to the simulator to evaluate different architectural tradeoffs in terms of metrics. Then, the Design Space Exploration framework can be used to sail over architectural solutions following several heuristic optimisation algorithms. This step is implemented as an optimisation loop, where the selected architecture instance generated by the DSE framework is given back to the estimation framework for the metrics evaluation. The tool integration phase in MULTICUBE enabled to implement an automatic system optimisation engine to generate, for the target MPSoC architecture, either the best architectural alternative (if the exploration is done at design-time) or the best tasks scheduling and allocation solution (if the exploration is done at run-time).

MULTICUBE* *will focus on multi-objective design space exploration for embedded System-on-Chip architectures

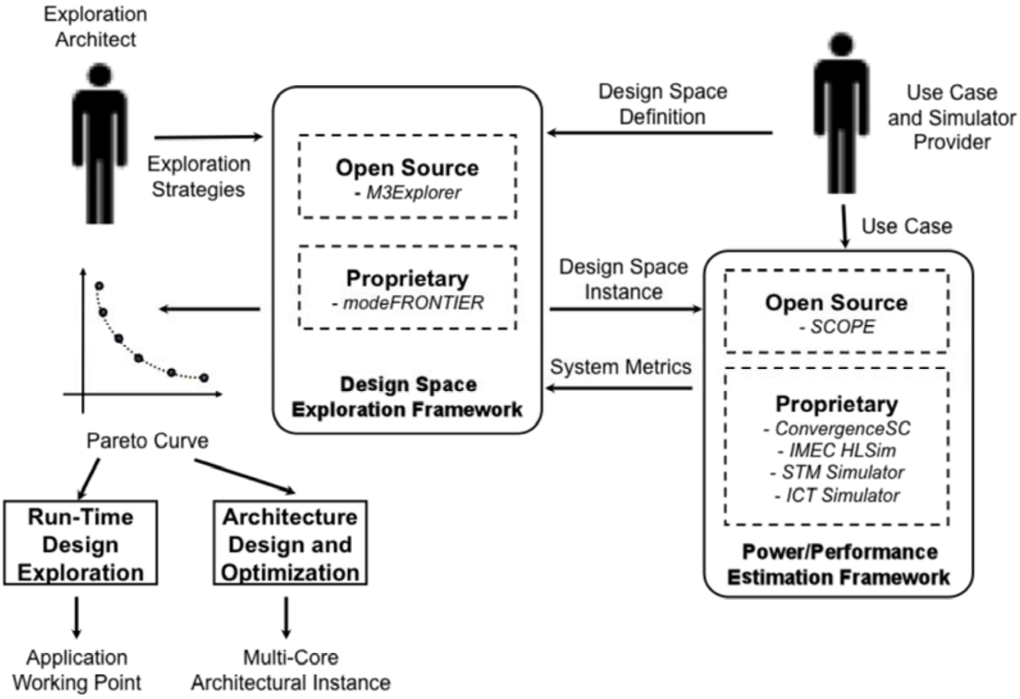
Summary of MULTICUBE Objectives

- Innovative design-time and run-time design exploration methods to increase system development productivity while achieving predictable system properties, particularly cost, performance and power consumption.
- To establish a strategic cooperation with China, by including ICT - Chinese Academy of Sciences and STMicroelectronics Beijing as strategic partners from a region with the fastest economy growing rate and technology market for consumer electronics.
- Integrated design tool suite that responds to the needs of industry for designing and prototyping embedded systems.
- Increased interoperability of tools from SME vendors as a general-purpose design exploration tool will be applied for embedded systems design.
- Development of an open tool framework facilitating new entrants and the integration of the tool chain including associated standardization.
- Development of multi-level optimized tools respecting trade-offs when co-developing hardware and software.

MULTICUBE Exploitable Results

At the end of the project, the MULTICUBE objectives have been successfully reached in terms of the following Exploitable Results:

1. An **Automatic Design Space Exploration Flow** for complex architectures such as Multiprocessor Systems on Chip designed for embedded computing applications The DSE flow is based on the interaction of two frameworks to be used at design time: the Design Space Exploration Framework (developed in **WP3**), an architecture exploration set of tools, and the Power/Performance Estimation Framework (developed in **WP2**), a set of modelling and simulation tools operating at several levels of abstraction. The DSE flow also includes a Run-time Resource Manager able to select at run-time the best design alternatives in terms of power/performance trade-offs generated during the design-time exploration phase. According to the exploitation plan defined in **WP5,** the MULTICUBE design flow is based on the co-existence of the open-source and the proprietary exploitation models. Based on this twofold exploitation plan, in the DSE flow co-exist open-source prototype tools and proprietary tools developed by the project partners. The design flow proved the great potential of the concept of integrating different tools adopting a **common standard interface.** The concept of the MULTICUBE design flow has been implemented in an **Integrated Design Tool Prototype** and validated on several industrial use cases in the final validation phase of the project.

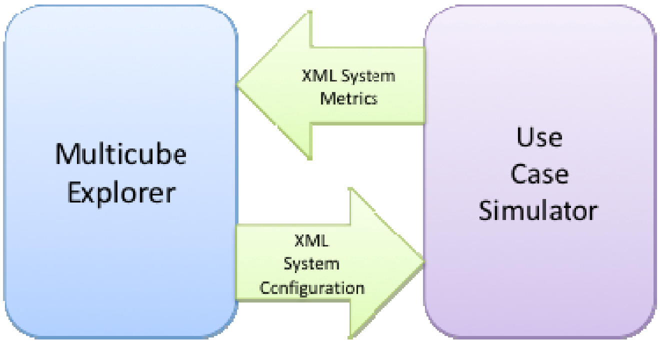


MULTICUBE Design Flow

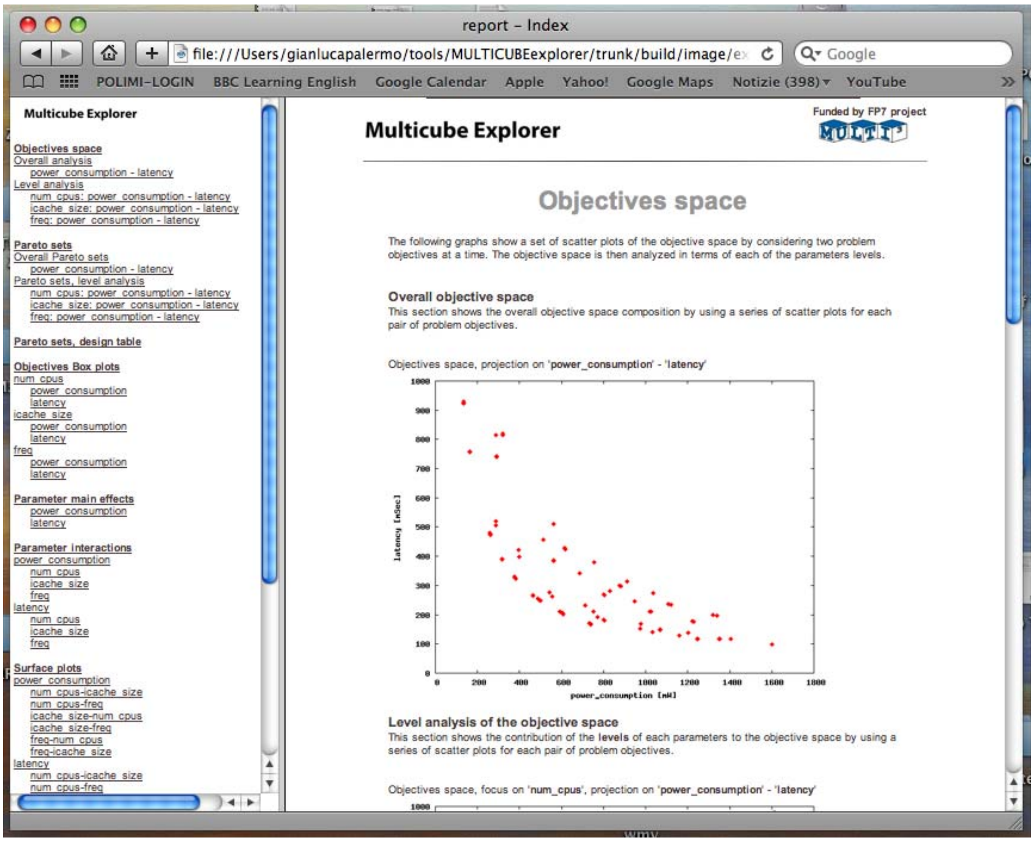
2. A **Design Space Exploration Framework:** an architecture exploration set of tools able to suggest to the designers the most appropriate optimisation of the multi-processor SoC considering several figures of merit such performance and energy consumption. The Design Space Exploration tools – developed in **WP3** – can be used at design time to automatically identify the Pareto optimal solutions in a multi-objective exploration given a set of design space

parameters. During the MULTICUBE project, two design space exploration tools and some optimisation and analytical techniques have been developed and validated.

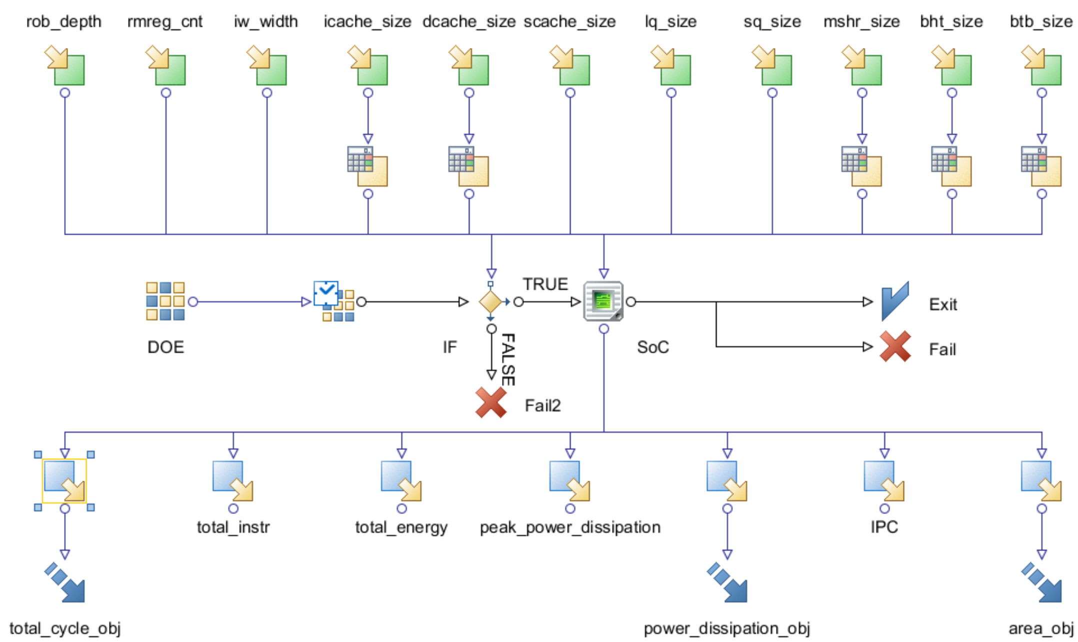
2.1. A new **open source tool (MULTICUBE Explorer,** in short **M3Explorer**) suitable for automatic design space exploration of MPSoC architectures. The tool enables a fast optimisation of parameterized system architecture towards a set of objective functions (e.g., energy, delay and area), by interacting with a system-level simulator through an open **XML-based interface**.



M3Explorer provides a set of innovative sampling and optimisation techniques to support the designer in finding the best objective-function trade-offs. It also provides a set of Response Modeling Methods for speeding up the optimisation phase. The prototype version of M3Explorer open-source tool has been released as **D3.1.2** and it is available at the Open Source page of MULTICUBE web site to guarantee a wide exploitation and dissemination of the MULTICUBE research. The interest towards M3Explorer has been proved by 465 tool downloads in the last two years. The main vehicle for the future exploitation of M3Explorer is represented by its adoption as part of the design flow in several international research projects. Among them, M3Explorer is currently used in three on-going European projects: FP7-COMPLEX IP, FP7-2PARMA STREP and ARTEMIS-SMECY. As further research exploitation actions, M3Explorer interfaced to IMEC HLSim simulator has been introduced in the IMEC tool chain to support design space exploration at design-time and run-time.

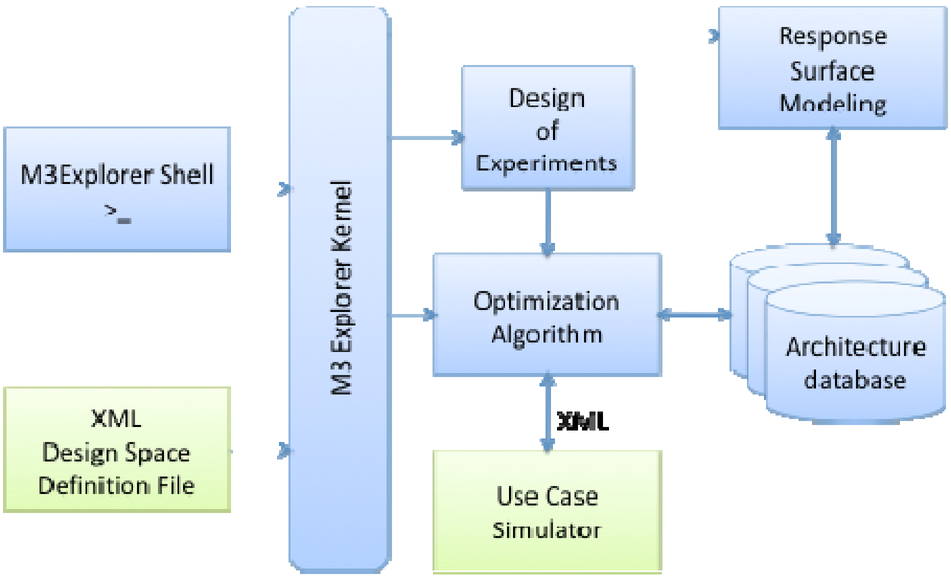


2.2. An existing commercial tool **(modeFRONTIER from ESTECO),** widely adopted in other optimisation fields, has been retargeted to support automatic DSE in the embedded systems field. The tool includes the most recent optimisation techniques available in literature, ranging from Design of Experiments to direct optimisers. modeFRONTIER (see also http://www.esteco.com) provides meta-modelling support for the creation of interpolating surfaces from well statistically distributed designs to be used to perform the optimisation without computing any further analysis. The tool also supports multivariate statistical analysis and data mining tools directly integrated in the exploration process to enable the user to easily analyse complex data. The graphical user interface of modeFRONTIER provides access to all features of design experiment definition, exploration and analysis in a simple and intuitive way. The complete set of tools developed by ESTECO in the MULTICUBE project has been included into **modeFRONTIER 4.3** which has been delivered in beta version to modeFRONTIER users in June 2010, and distributed as official commercial release at the end of October 2010. The official presentation of the new features included in the SoC integration node took place during the last modeFRONTIER International Users' Group Meeting held on May 2010 in Trieste, Italy. The integration of the SoC library developed in MULTICUBE project into the new commercial release of **modeFRONTIER 4.3** represents one of the most significant exploitation results of the project. This would potentially enable to position ESTECO (an Italian SME active since more than ten years basing its business on multidisciplinary industrial design optimisation) as one of the fewer European players in the embedded systems' EDA market worldwide.



2.3. **A set of multi-objective optimisation algorithms,** representing the core of the exploration process, has been developed and validated on some industrial use cases. In multi-objective optimisation problems there are more than one objective to be optimised (maximized or minimized), meaning that the outcome of the optimisation process is not a single solution but a set of solutions. This set of solutions, which is called the Pareto front, represents the tradeoffs between the different (and possibly contradictory) objectives. The set of algorithms implemented includes state-of-the-art algorithms widely used in the field of multi-objective optimisation (ranging from evolutionary and genetic algorithms up to simulated annealing and particle swarm algorithms), enhanced versions of algorithms that were specifically targeted in the project for the multi-core SoC design, and new developed algorithms. Results of the optimisation algorithms developed and/or re-engineered during the project have been released as **D3.2** Public Document at the MULTICUBE web site for public dissemination and exploitation purposes.

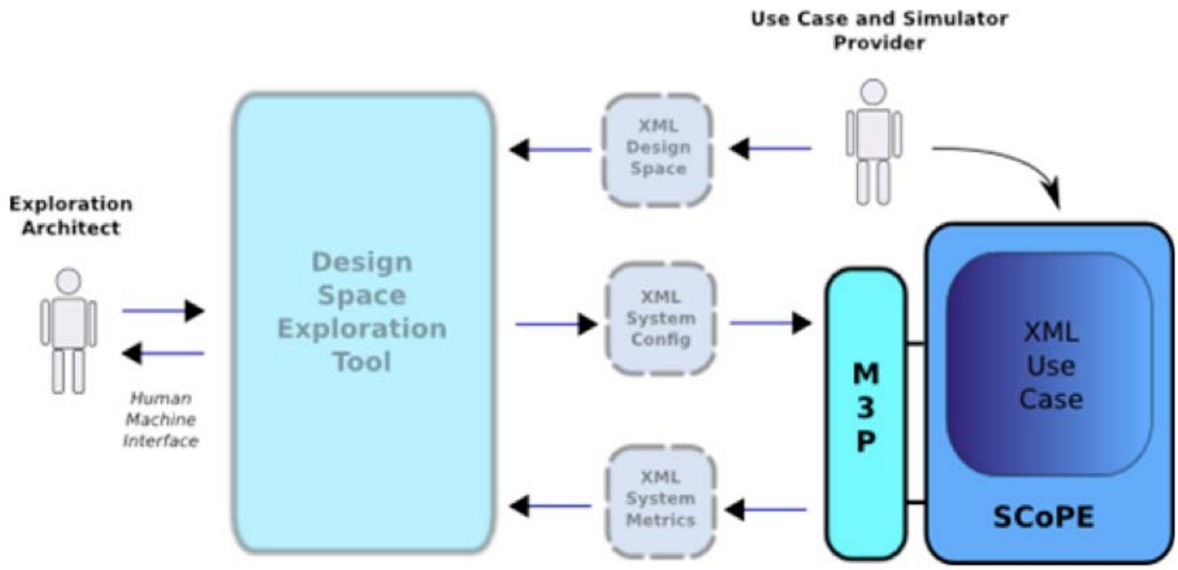
2.4. **Analytical techniques (Response Surface Models, RSMs)** to speed up the design space exploration process have been developed to model the system behaviour without requiring the simulation of all the possible design configurations. RSMs have been proved to be an effective solution for analytically predicting the behaviour of the system in terms of the target metrics without resorting to the system simulation. Response Surface Modelling (RSM) techniques leverage the analytical dependence between several design parameters and one or more response variables adopting both interpolation and regression techniques. The working principle is to use a set of simulations either generated ad hoc by a Design of Experiment (DoE) phase or obtained by an exploration strategy previously applied to the design space, in order to obtain a response model. A set of analytical techniques (Shepard interpolation, radial basis functions, linear regression, artificial neural networks and Spline-based regression) have been implemented as software modules and integrated in M3Explorer open-source tool. Results of the application of RSM techniques are publicly available in **D2.3.2** at the MULTICUBE web site for future dissemination and exploitation.



Structure of M3Explorer tool

3. **A Power/Performance Estimation Framework** (methodology and related tools) has been set up to provide accurate estimates for complexity, timing and power consumption at different abstraction levels and for different use cases. A set of tools – developed in **WP2** – has been used for the system modelling and estimation of several metrics such as energy consumption and execution time of the target MPSoC platforms:

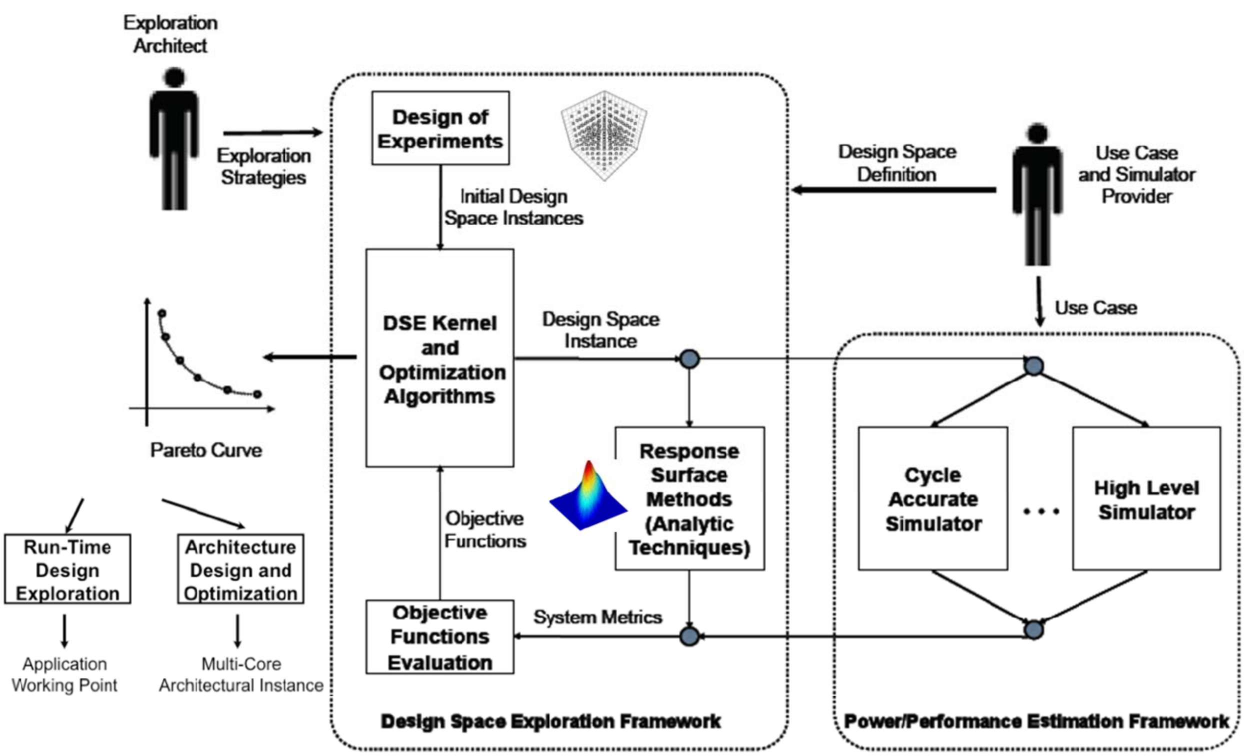
   3.1. **MULTICUBE-SCoPE**, the extension of the open-source high-level SCoPE performance and power evaluation framework. The tool can accept complex system descriptions and it can dynamically generate the system models considering the configuration parameters received from the DSE tools. Then, the tool can feed back the required system metrics to the DSE engine. The prototype version of MULTICUBE-SCoPE (released as **D2.1.2**) is available at the Open Source page of MULTICUBE web site for a broad dissemination and exploitation action. The main vehicle for the future exploitation the tool is also represented by its usage as modelling and simulation purposes in several upcoming research projects: SCALOPES (SCAlable, Low Power Embedded PlatformS, Artemis, n.100029), COMPLEX (Co-design and power management in platform based design space exploration, IP project n.24799) and ESA - HW/SW Codesign (ESA TEC-SWE/08-167/EC). As a consequence, the results obtained in the MULTICUBE project will be delivered to a wider scientific and industrial community.



   3.2. A proprietary set of simulation tools developed by IMEC as SystemC-based **Transaction-Level** Multi-core simulator built on top of the CoWare virtual prototyping environment to support platform-based design approach. The TLM-based prototype simulator has been released as **D2.2.2** and it is integrated with both modeFRONTIER and M3Explorer tool.

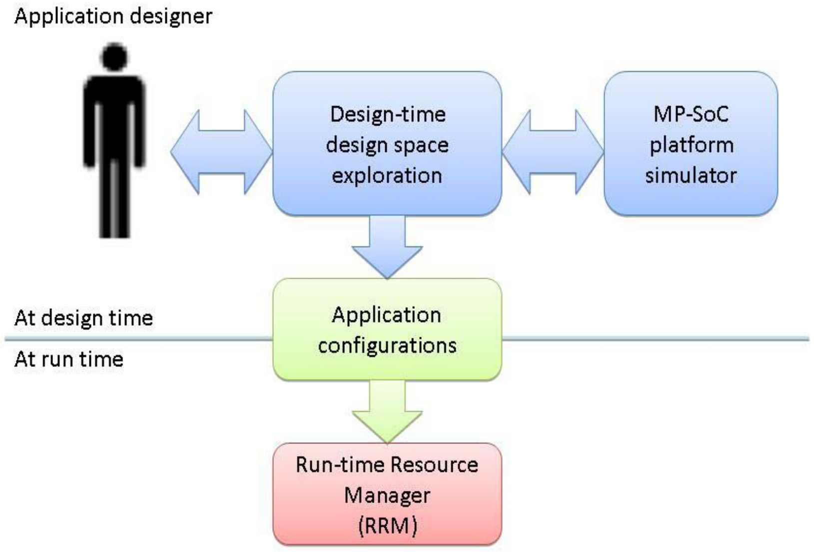
   3.3. A high-level time-annotated simulator **(HLSim, developed by IMEC)** to provide a fast simulator at higher abstraction levels to estimate the metrics like performance and power consumption for a given platform architecture executing a parallelized version of the application. During MULTICUBE project, HLSim extended with metrics on energy consumption has been used for the multimedia use case to do a relative comparison between different architectures and parallelisations. The introduction of HLSim in the design flow had as benefit the speed up of the multimedia use case simulation and to start the design exploration experiments earlier than planned. HLSim-based explorations are much faster than TLM-based ones so as more extensive DSE was done by using HLSim to extract Pareto set information to be used at run-time. Cross validation of the results obtained by using HLSim and TLM-based simulation on the multimedia use case has been carried out during the validation phase of the project (**WP4**).

4. The MULTICUBE Consortium has developed a methodology (the **Multi-Simulator based DSE Approach**) to avoid potentially sub-optimal DSE results based on using multiple platform simulators to run the application at different abstraction levels. The main idea is to measure timing information (in terms of processor cycles) for an application execution on an accurate simulator (e.g. TLM-based cycle-accurate simulator) and feed this timing information back to high-level timed simulations (e.g. HLSim) to achieve validation across simulators. Then, an exhaustive DSE is done with a large set of application runs by using faster higher-level simulators (e.g. HLSIm) and then the derived interesting operating points (usually clusters of operating points) are explored by using more accurate simulators (e.g. TLM-based and/or cycle-accurate simulators). The proposed methodology exploiting the synergy of multiple simulators at several abstraction level can be used to further speed up the DSE process while guaranteeing the accuracy of the simulation results. The methodology has been validated for the MPEG4 encoder application provided by IMEC by using three different simulators (M3SCoPE, HLSim and TLM-based simulator) interfaced with the two available DSE tools (modeFRONTIER and M3Explorer). The Multi-Simulator based DSE Approach is fully described in the public deliverable **D4.2.4** available at the MULTICUBE web site.



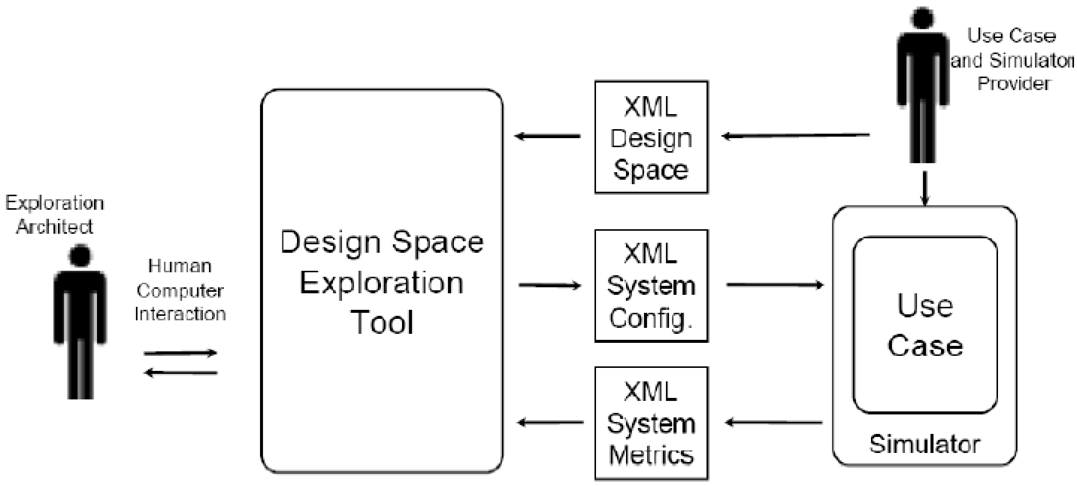
Detailed view of MULTICUBE Design Flow based on multiple simulators at several abstraction levels and analytic techniques

5. *At design time,* the multi-objective design space exploration framework generates a set of Pareto-optimal operating points (for every application) annotated with system metrics like energy consumption, execution time, and memory and communication bandwidth values. The Pareto set can then be exploited *at run time* (while the application(s) are running) to optimise the overall system behaviour. Specifically a separate **Run time Resource Manager (RRM)** has been developed to exploit the set of operating points derived at design-time for all applications to steer the overall system behaviour according to the imposed user requirements (quality, power, performance, etc.). The goal of the RRM is to use the Pareto information given by the design-time exploration on the operating points (of all the applications) to make at run-time a decision to allocate the resources to active applications based on the user requirements in term of Quality of Service. Being part of the IMEC IP portfolio, the Runtime Resource Manager represents one of the most important exploitable results of MULTICUBE project. The basic concepts and the methodology related to the RRM are described in the Public Deliverable **D3.3.2** and in some recent scientific papers listed as Public Documents at the MULTICUBE web site.



MULTICUBE Exploration Framework for Runtime Resource Management

6. Starting from the definition of MULTICUBE design flow, a great effort has been dedicated to the development of an **Integrated Design Tool Prototype** based on the co-existence of open-source and proprietary tools. The integrated design flow has then been proven on several industrial use cases in the final validation phase of the project. The prototype has been released as a **Linux Virtual Machine** including all the MULTICUBE tools pre-installed and ready to be executed (as described in the Confidential Deliverable D1.4.2). The main goal of the prototype is to provide an integrated environment in the forms of ready-to-use executable software from which all the tools developed in the project can be evaluated together – even after the end of the project – without the need of any software installation procedure. The Confidential Deliverable D1.4.2 is available to project partners to facilitate their future internal exploitation of the MULTICUBE design flow. Anyway a reduced design tool prototype in the form of **a public demonstrator** of a multimedia application and related documentation is available at the MULTICUBE web site (and released as D4.2.3) for external dissemination and exploitation purposes. The public demonstrator is based on the multimedia use case provided by IMEC using an MPEG4 encoder IP modelled and optimised by exploiting **MULTICUBE open-source technology and tools** (MULTICUBE-SCoPE and M3Explorer).
   6.1. Strategic importance from the point of view of the MULTICUBE exploitation is associated to the **common XML Tool Interface Specification** for the integration of the different tools and use cases. The common interface enables the independent development of modules and a seamless integration of the design tools and the data structures into a common design environment. The specification is defined in terms of XML, a widely used standard notation. The XML interface has been originally defined in Deliverable **D1.4.1.** Afterwards the updated **MULTICUBE XML Interface Specification Release 1.4** has been exploited as Public Document on the MULTICUBE web site. In this way any performance evaluation tool, provided by any third party but compliant with the defined interface, can potentially exploit the advantages offered by the MULTICUBE design flow.



The goal of XML interface is to formally define the interaction between the simulator and the design space exploration tools, which is essentially an automatic program-to-program interaction. In general, the interaction can be described as following. First, the design space exploration tool automatically generates to the simulator one feasible system configuration whose system metrics should be estimated by the simulator. Second, the simulator generates a set of system metrics to be automatically fed back to the design space exploration tool. This specification provides an XML based grammar for writing both the design space definition file and the simulator interface files. We define the interface between the Design Space Exploration Tool and the Exploration Architect as the human-computer-interaction interface. This interface can be GUI (Graphical User Interface)-based or command-line-based and it is used for specifying and solving the exploration problem in terms of optimisation metrics and constraints. STMicroelectronics is willing to study the possibility of an IP-XACT extension for Design Space Exploration by the inclusion of the main features of the MULTICUBE XML Interface Specification Release 1.4.

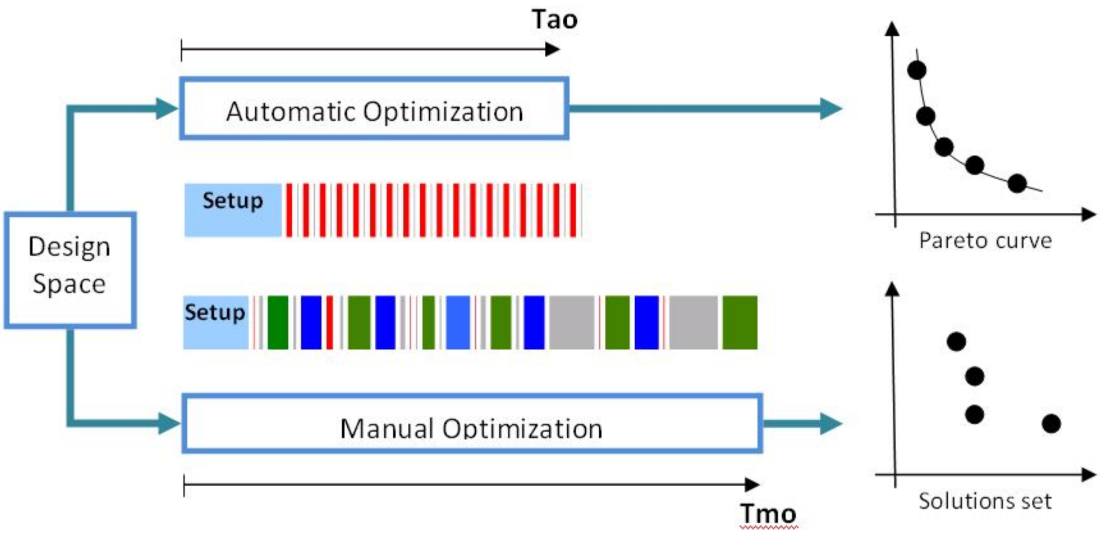
6.2. The Deliverable D1.4.2 provides an executable software environment **(Validated Prototype of Integrated Design Tool)** that includes all the software tools developed in the MULTICUBE project. Particular attention has been dedicated to integration aspects, so the deliverable can be considered more as a unified set of tools than just a simple set of independent software components. Emphasis on integration is presented through a collection of integrations examples (**Demonstrators**). The prototype has been implemented as a Linux Virtual Machine, with all the MULTICUBE software tools pre-installed and ready to be executed. Then the integrated prototype has been used during the project validation phase.

7. The benefits of the introduction of the Automatic DSE in the design phase of embedded computing systems (justifying its introduction in industrial design processes) have been assessed trough a procedure described in **D4.1.2** “Final Evaluation Plan” and afterwards exploited in the Public Deliverable **D4.2.4** “Final report on application of MULTICUBE design flow to the demonstrators”. The **Automatic DSE Assessment Procedure** addresses the final objective design quality and the reduction of design turn around time by introducing such a technology on the entire design process. The benefits on the design process can be measurable and tangible like the reduction of the overall design process lead time, and qualitative or intangible like the streamlining and the reduction of human error prone repetitive operations. The DSE assessment procedure was the basis for the validation of each of the use cases of the project. Validation results have been assessed based on a set of common assessment criteria.

8. Four **Use Cases** (defined as combination of application and related architecture) combined with the two exploration tools in several different validation paths have been used to assess the capabilities of the MULTICUBE design flow and tools in an industrial design process. **Three demonstrators** (DS2 Powerline, STM-SP2 Low-Power Processor, and ICT Multi-core Architecture) are confidential and they can be directly accessed by project partners for internal exploitation purposes of the MULTICUBE design framework and related results. The use cases provided by the industrial partners are actual models of future products or families of products. They have been optimised through the MULTICUBE methodology. At the end of the project, parameters for optimising the architecture of each use case are available to each use case provider, for a direct exploitation of MULTICUBE outcomes for further internal design activities Anyway a **public demonstrator** based on the multimedia use case using an MPEG4 encoder application is also available at the Open Source page of MULTICUBE web site (and released as D4.2.3) to facilitate a broad external exploitation of MULTICUBE technology and for training purposes. The public demonstrator is based on the multimedia use case provided by IMEC using an MPEG4 encoder IP modelled and optimised by exploiting **MULTICUBE open-source technology and tools** (MULTICUBE-SCoPE and M3Explorer). Note that *two out of four final*

project demonstrators are related to use cases provided by Chinese partners (STMicroelectronics Beijing and ICT - Chinese Academy of Science) demonstrating the fruitful cooperation established with them. This collaboration opens interesting exploitation challenges of MULTICUBE project results in a region with the fastest economy growing rate and a wide technology market.

Phases of automatic and manual optimizations



Comparison between automatic and manual optimisations

Testimonials:

DS2: *"The proposed flow can save up to 80% of designer time while achieving better results in terms of performance since much more simulations can be run and analysed following this flow obtaining ten times more possible combinations than with the semi-automatic design flow".*

STMicroelectronics: *"The use of MULTICUBE optimisation flow can save up to a 73% of the overall time and achieving comparable results in terms of power/performance tradeoffs…. The overall conclusion of the utilization of MULTICUBE design flow over a real industrial use case like the one just discussed is that the added value overcomes largely the cost of setting up the whole process, converging much faster to the optimum solution for a given technical problem."*

IMEC: *"Looking at the two design space exploration case-studies, it can be seen that using automatic DSE over manual full-space exploration has large benefits in terms of time-to-market and accuracy of exploration results. By using automatic DSE in dynamic runtime management evaluation case-study, design space exploration time was reduced from 6 months (full-space) to 36 hours. In another case-study of MPSoC platform optimisation, by using a simulator at higher abstraction level coupled with automatic DSE, we could reduce design space exploration time from worst case of 153 years (full-space) to 36 hours… The extra efforts required to build automatic DSE procedure were minimal".*