MULTICUBE

Project Coordinator
Name: ***Cristina Silvano***
Institution: ***Politecnico di Milano***
Email: ***silvano@elet.polimi.it***

Project website:
`www.multicube.eu`

Partners:
Politecnico di Milano (Italy),
Design of Systems on Silicon – DS2 (Spain),
STMicroelectronics (Italy),
IMEC (Belgium),
ESTECO (Italy),
University of Lugano - ALaRI (Switzerland),
University of Cantabria (Spain),
STMicroelectronics Beijing (China),
Institute of Computing Technology – Chinese Academy of Sciences (China)

Duration: ***30 months***
Start: ***2008.01.01***
Contract Number: ***INFSO-ICT-216693***

MULTICUBE

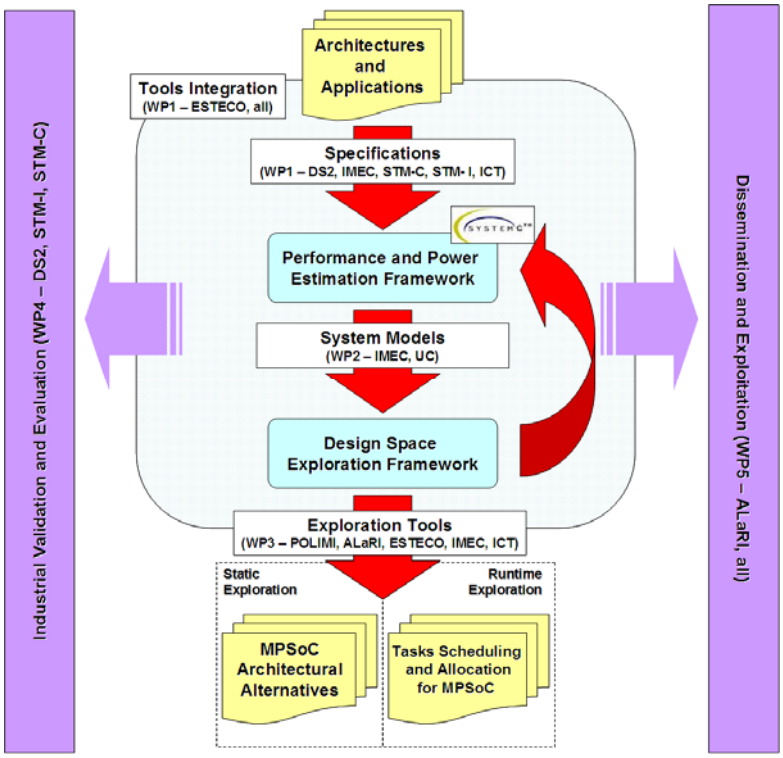
MULTI-OBJECTIVE DESIGN SPACE EXPLORATION OF MULTI-PROCESSOR SOC ARCHITECTURES FOR EMBEDDED MULTIMEDIA APPLICATIONS

Many point tools exist to optimize particular aspects of embedded systems. However, an overall design space exploration framework is needed to combine all the decisions into a global search space, and a common interface to the optimization and evaluation tools. The MULTICUBE project focuses on the definition of an automatic multi-objective Design Space Exploration (DSE) framework to be used to tune the System-on-Chip architecture for the target application evaluating a set of metrics (e.g. energy, latency, throughput, bandwidth, QoS, etc.) for the next generation of embedded multimedia platforms. This overall objective is two-fold.

From one side, the MULTICUBE project will define an automatic multi-objective DSE framework to find design alternatives that best meet system constraints and cost criteria, strongly dependent on the target application, but also to restrict the search space to crucial parameters to enable an efficient exploration. In the developed DSE framework, a set of heuristic optimization algorithms must be defined to reduce the overall exploration time by computing an approximated Pareto set of configurations with respect to the selected figures of merit. Once the approximated Pareto set has been built, the designer can quickly select the best system configuration satisfying the constraints.

From the other side, the MULTICUBE project will define a run-time DSE framework based on the applications of the results of the static multi-objective design exploration to optimize the run-time allocation and scheduling of different application tasks. The design exploration flow results in a Pareto-optimal set of design alternatives with different speed, energy, memory and communication bandwidth parameters. This information can be used at run-time by the operation system to make an informed decision about how the resources should be distributed over different tasks running on the multi-processor system on-chip. This resource distribution cannot be performed during the design exploration itself, since it depends on which tasks are active at a particular point in time.





MULTICUBE tool environment and design flow linked to the five workpackages

The goal of MULTICUBE is to cover the gap between the system-level specification and the definition of the optimal application-specific architecture. MULTICUBE activities are driven by the idea to cover this gap by building a stack of tools and accurate methodologies directly targeted to specific multi-core architectures. In the MULTICUBE design flow, the specifications of the target architectures and applications will be provided as inputs to the design flow.

A SystemC-based multi-level modeling methodology for multiprocessors will be developed. Once received the target architecture as input, we will provide to the next step the system model to evaluate different architectural alternatives in terms of metrics. Then, the Design Space Exploration framework will be defined to sail over architectural solutions following several heuristic optimization algorithms. This step is implemented as an optimization loop, where the selected architecture instance generated by the DSE framework is given back to the estimation framework for the metrics evaluation. The tool integration phase in MULTICUBE will be performed to implement an automatic system optimization engine to generate, for the target MPSoC architecture, either the best architectural alternative (if the exploration is done statically) or the best tasks scheduling and allocation solution (if the exploration is done at run-time)

MULTICUBE will focus on multi-objective design space exploration for embedded System-on-Chip architectures

Summary of MULTICUBE Objectives

- Innovative static and run-time design exploration methods to increase system development productivity while achieving predictable system properties, particularly cost, performance and power consumption.
- To establish strategic cooperation with China, by including ICT - Chinese Academy of Sciences and STM - China as strategic partners from a region with the fastest economy growing rate and technology market for consumer electronics
- Integrated design tool suite that responds to the needs of industry for designing and prototyping embedded systems.
- Increased interoperability of tools from SME vendors as a general-purpose design exploration tool will be applied for embedded systems design;
- Development of an open tool framework facilitating new entrants and the integration of the tool chain including associated standardization.
- Development of multi-level optimized tools respecting trade-offs when co-developing hardware and software

Key Issues

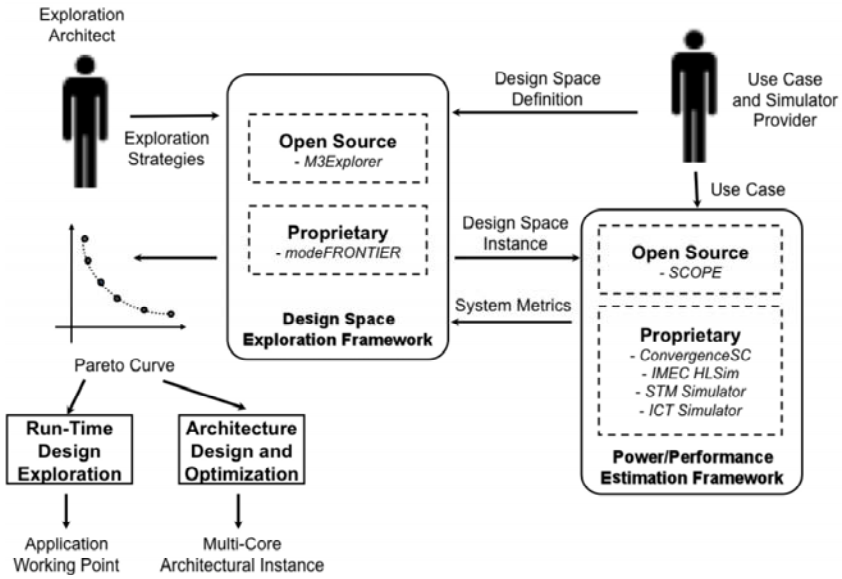
- Increased productivity of system development through a fast, reliable DSE process allowing finding an optimized solution in a short time. DSE will be performed at system-level, thus avoiding costly, low-level analysis steps (i.e. ISS simulations).
- Improved competitiveness of European companies that rely on the design and integration of embedded systems in their products by reducing costs and time to market.
- Stimulate high-tech European SMEs (such as ESTECO) that offers general-purpose innovative design solutions and tools to apply them for embedded systems design.
- Reinforced European scientific and technological leadership in the engineering of complex systems both at the industry side (STM as a large company and DS2 as a SME) and the academic and research side (IMEC, Politecnico di Milano, ALaRI, University of Cantabria and Institute of Computing Technology).

Expected Impact

The MULTICUBE design methodology is implemented at system-level in a set of open-source and proprietary EDA tools to guarantee a large exploitation of the results of the MULTICUBE project in the embedded system design community. The overall goal is to support the competitiveness of European industries by optimising embedded HW/SW systems while reducing the design time and costs. To ensure a wide applicability of the proposed DSE framework, the MULTICUBE project is strongly industry-driven. Two European industrial partners (STM Italy and DS2) and STM China have defined the requirements of the design tools and they will validate step-by-step the results of the exploration tools to design a set of target industrial applications. The integration of design tools and the commercial exploitation of the tools are in charge of an European SME, ESTECO. ALaRI is mainly in charge of dissemination and exploitation activities. The research and technological development are carried out by IMEC, Politecnico di Milano, University of Cantabria and the Institute of Computing Technology.

The MULTICUBE Design Flow

During the first year, the overall MULTICUBE design flow has been defined to support the automatic Design Space Exploration (DSE) of embedded systems.

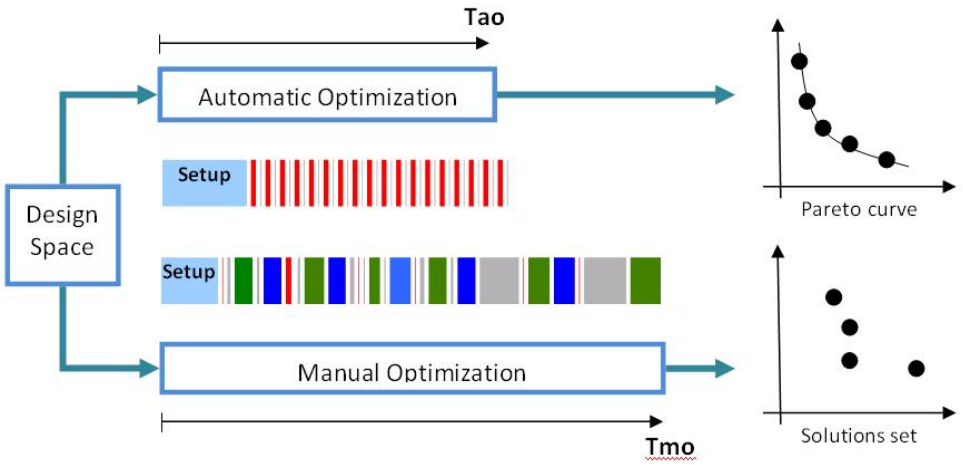


MULTICUBE Design Flow

The MULTICUBE design flow is based on two main frameworks: the *Design Space Exploration Framework* (developed in **WP3**) and the *Power/Performance Estimation Framework* (developed in **WP2**). According to the exploitation plan defined in **WP5,** the design flow is based on the synergy of the open-source exploitation model and the proprietary exploitation model. According to this twofold exploitation plan, in the DSE framework there are the open-source M3Explorer prototype tool and the modeFRONTIER proprietary tool provided by ESTECO. Similarly, the Power/Performance Estimation Framework is based on two different sets of open-source and proprietary tools developed by the project partners. Two types of users can interact with the MULTICUBE design flow. From one side, the Use Case Simulator Provider is the user in charge of giving the executable model of the target architecture and application. The target architecture must be configurable in terms of a set of design space parameters. From the other side, the Exploration Architect defines the exploration strategies to be used to identify the set of Pareto points corresponding to the optimal architecture configurations and application working points. Once obtained the design space definition, the DSE framework starts an optimisation loop interacting with the estimation framework in order to find the optimal system configurations in terms of the target power/performance metrics. In the optimisation loop, the DSE Framework generates the next design space instance to be simulated to obtain an estimate of the system metrics. In the automatic loop, the system metrics are fed back to the DSE tool to refine the exploration process. Once the design space exploration process terminates, the resulting set of Pareto points are provided to the system architect representing the multi-objective trade-offs. If the set of configurable parameters contains also a set of parameters related to the application, the approximated Pareto set generated by the Design Space Exploration Framework is taken as input from the Run-Time Design Space Exploration module to select the application working point meeting the constraints.

Description of the work performed in Year 2 (Second Reporting Period)

Starting from the MULTICUBE design flow defined during the first year, the main effort of the second year has been dedicated to the development of an integrated design flow based on the co-existence of open-source and proprietary tools **(WP1).** More in detail, the activities in **WP2** has mainly been focused during the last year on the release of the prototype of the open-source M3-SCoPE framework, the internal release of the transaction-level multi-core simulation environment and the definition of the analytic techniques to significantly reduce the exploration time. In this second reporting period, the **WP3** efforts have been concentrated on the release of the open-source M3Explorer prototype and the retargeting of modeFRONTIER tool for the optimization of embedded Systems-on-Chip. Some effort has also been spent on the implementation and evaluation of new optimization algorithms in modeFRONTIER and M3Explorer tools. During the last six months, some activities started in **WP3** on the definition of *run-time* design space exploration techniques based on the Pareto information obtained from the design-time exploration to optimize at run-time the task allocation and scheduling. During the second year, a strong effort has been spent by all partners in **WP4** on the definition of the final validation plan after step-by-step validation to enable entering in the final validation phase during the next six months. Moreover, the strategic cooperation with Chinese partners has been reinforced. Staring from the initial dissemination and exploitation plans defined at the end of the first year, the partners concentrated on dissemination and dissemination activities to enforce the European scientific and technological leadership in the engineering of complex systems both at the industry side (STM as a large company and DS2 and ESTECO as a SME) and the academic and research side (IMEC, Politecnico di Milano, ALaRI, University of Cantabria and Institute of Computing Technology).
Overall, at the end of the second reporting period, the project maintained its promises and it is ready to enter the final validation phase. By the end of the project, we're confident that the project will improve the development of multi-processor Systems-on-Chip through an efficient automatic DSE process that allows finding a set of Pareto optimized design solutions. The Pareto set is automatically identified in a shorter time with respect to a conventional design flow where the optimization process is done manually, based on designer ability and past experience to assess the simulation results and to move towards the next instance of the model to be simulated.



Comparison between automatic and manual optimization

Phases of automatic and manual optimization

Main Achievements of Year 2 (Second Reporting Period):

- Development of the integrated MULTICUBE design flow to support the automatic DSE after the completion of step-by-step validation **(WP1-WP4).**
  - Release of the open-source prototype tool **(M3-SCoPE**) for performance and power estimation **(WP2).**
  - Internal release of Transaction-Level and High-Level Simulators for the Multimedia Use Case **(WP2).**
  - Release of the open-source prototype design space exploration framework **(M3 Explorer) (WP3).**
  - Retargeting of **modeFRONTIER** optimization tool to the discrete domain to be used in the embedded systems field **(WP3).**
- Definition of final validation plan after the step-by-step validation **(WP4):**
  - Definition of assessment procedures including: progress monitoring procedure, milestones assessment procedure and automatic DSE assessment procedure.
  - Update of the requirements of the design tools **(WP4).**
  - Update of the specification for the design flow integration **(WP4).**
  - Update of the specifications of the industrial use cases **(WP4).**
- Definition of a *run-time* design exploration framework **(WP3).**
- Reinforcement of the strategic cooperation with Chinese partners **(WP3-WP4).**
- Update of the initial dissemination and exploitation plans **(WP5)**